REMARKS

Applicant wishes to thank the Examiner for taking time to conduct a courteous and very professional personal interview on January 15, 2003, with Applicant's representative. It is felt that this interview was very beneficial to advance prosecution.

Attached hereto is a marked up version of the changes made in the claims by the current Amendment. The attached page is captioned "**Version with markings to show changes made.**"

It is noted that the claim amendments herein are intended solely to more particularly point out the present invention for the Examiner, and not for distinguishing over the prior art or the statutory requirements directed to patentability. It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Claims 1, 2, 4, 5, and 14-24 are all of the claims pending in the present Application. New claims 15-24 are added.

Claim 14 is allowed, upon providing a new declaration for this claim. Claims 1, 2, 4, 5 stand rejected under 35 USC §103(a) as unpatentable over US Patent 6,096,648 to Lopatin et al. taken in combination with US Patent 6,037,664 to Zhao et al.

These rejections are respectfully traversed in view of the following discussion.

I. The Claimed Invention

As described and claimed, for example by claim 1, the present invention is directed to a semiconductor device including a first interlayer insulating layer. A plurality of wiring lines, which are formed of Cu whose concentration is equal to or higher than 10^{19} atoms/cm^3, is formed on the first interlayer insulating layer. An insulating layer which has a property that Cu is unlikely to enter insulates between the plurality of wiring lines. A second interlayer insulating layer is on the insulating layer having a property that Cu is unlikely to enter therein and the plurality of wiring lines.

That is, as clearly shown in Figures 6A-6P, in one preferred embodiment, each HSQ layer 3, 9 has a lower interlayer insulating layer 2,8 and an upper interlayer insulating layer

7,13 to provide reinforcement to offset the lower strength of the HSQ layer.

II. The Prior Art Rejection

The Examiner asserts that US Patent 6,096,648 to Lopatin et al., in combination with US Patent 6,037,664 to Zhao et al., essentially teaches the invention as described by claims 1, 2, 4, and 5. Applicant respectfully disagrees.

A key feature of the present invention is that each HSQ layer has an insulative layer both above it and below it. That is, in the embodiment shown in Figure 6P, HSQ layer 3 has lower insulative layer 2 and upper insulative layer 7. HSQ layer 9 has lower insulative layer 8 and upper insulative layer 13. This feature provides an advantage that a strength of the HSQ layer is offset by the strength of the upper and lower insulative layers. Neither Lopatin nor Zhao teachs, suggests, or renders obvious this feature.

That is, as clearly shown in Figure 12 of Zhao, there is no interlayer insulation layer below HSQ layer 11, and there is one etch stop layer 13, 15, 19 respectively on top each of HSQ layer 11, 14, 18, where etch stop layer 13 is SiN and etch stop layers 15 and 19 are each SiO_2. Zhao clearly fails to teach each HSQ layer as having both a lower and upper interlayer to provide strength.

For Zhao to anticipate the present invention, it would have to be modified to incorporate a layer for strength below layer 11 and would have to incorporate a second layer 13 and a second layer 15. Since layers 13,15 are used as an etch stop rather than compensation for strength, one of ordinary skill in the art would not reasonably add a second layer. Nothing in Lopatin overcomes this deficiency of Zhao.

Hence, turning to the clear language of the claims, there is no teaching or suggestion of "... a first interlayer insulating layer ... an insulating layer which has a property that Cu is unlikely to enter said insulating layer and which insulates between said plurality of wiring lines; and a second interlayer insulating layer on said insulating layer having a property that Cu is unlikely to enter therein", as required by independent claim 1.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

Further, the other prior art of record has been reviewed, but it too even in combination with Lopatin et al. and/or Zhao et al. fails to teach or suggest the claimed invention.

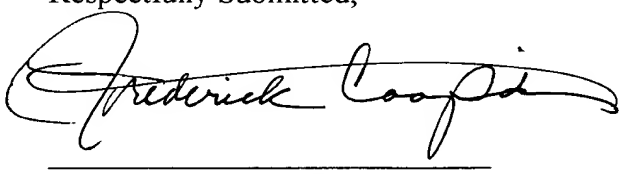
III. Formal matters and Conclusion

In view of the foregoing, Applicant submits that claims 1, 2, 4, 5, and 14-24, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,



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Frederick E. Cooperrider
Reg. No. 36,769

McGinn & Gibb, P.C.
8321 Old Courthouse Road, Suite 200
Vienna, Virginia 22182
(703) 761-4100
Customer No. 21254

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 1 and 4 have been revised, as follows.

1. (Amended) A semiconductor device comprising:

a first interlayer insulating layer;

a plurality of wiring lines which are formed of Cu whose concentration is equal to or higher than 10^{19} atoms/cm^3, said plurality of wiring lines formed on said first interlayer insulating layer;

an insulating layer which has a property that Cu is unlikely to enter said insulating layer and which insulates between said plurality of wiring lines; and

[at least one adhesion layer formed in an interface between said plurality of wiring lines and said insulating layer, said at least one adhesion layer allowing said plurality of wiring lines and said insulating layer to adhere to one another]

a second interlayer insulating layer formed on said insulating layer having a property that Cu is unlikely to enter therein.

4. (Amended) A semiconductor device according to claim 1, further comprising:

[a plurality of wiring lines which are formed of Cu whose concentration is equal to or higher than 10^{19} atoms/cm^3; and

an insulating layer which has a property that Cu is unlikely to enter said insulating layer and which insulates between said plurality of wiring lines; and]

at least one adhesion layer formed in an interface between said plurality of wiring lines and said insulating layer, said at least one adhesion layer allowing said plurality of wiring lines and said insulating layer to adhere to one another, [wherein said at least one adhesion layer has an etching rate which is essentially equivalent to an etching rate of said plurality of wiring lines,]

wherein each [of] said at least one adhesion layer has a polishing rate which is essentially equivalent to a polishing rate of said plurality of wiring lines.

The following new claims are added:

15. (New) A semiconductor device comprising:

a first interlayer insulating layer;

a first layer of low permittivity material formed on said first interlayer insulating layer, said low permittivity material having a property that a migration of copper is limited in said material;

a first plurality of sections of copper being embedded in said first layer of low permittivity material;

a second interlayer insulating layer formed on said layer of low permittivity material,

wherein said first interlayer insulating layer and said second interlayer insulating layer have a property in strength that offsets a property in strength of said first layer of low permittivity material.

16. (New) The semiconductor device of claim 15, wherein said first interlayer insulating layer and said second interlayer insulating layer each comprise SiN, and

said first layer of low permittivity material comprises hydrogen silsesquixane (HSQ).

17. (New) The semiconductive device of claim 16, further comprising:

a bottom layer formed below said first interlayer insulating layer, said bottom layer having at least one copper conductor line,

wherein said first interlayer insulating layer has a hole formed therein, said hole allowing at least one copper conductor line in said bottom layer to connect with one of said first plurality of sections of copper embedded in said first layer of low permittivity material.

18. (New) The semiconductor device of claim 17, further comprising:

a layer of adhesive material being formed at an interface between said first layer of low permittivity material and each of said first plurality of sections of copper being embedded therein.

19. (New) The semiconductor device of claim 18, wherein said adhesive material comprises tungsten (W).

20. (New) The semiconductor device of claim 15, further comprising:

a third interlayer insulating layer formed on said second interlayer insulating layer;

a second layer of low permittivity material formed on said third interlayer insulating layer, said low permittivity material having a property that a migration of copper is limited in said low permittivity material;

a second plurality of sections of copper being embedded in said second layer of low permittivity material; and

a fourth interlayer insulating layer formed on said second layer of low permittivity material.

21. (New) The semiconductor device of claim 20, wherein said first interlayer insulating layer, said second interlayer insulating layer, said third interlayer insulating layer, and said fourth interlayer insulating layer each comprising SiN, and

wherein said first layer of low permittivity material and said second layer of low permittivity material each comprises hydrogen silsesquixane (HSQ).

22. (New) The semiconductor device of claim 20, further comprising:

a layer of adhesive material formed at an interface between said second layer of low permittivity material and each of said second plurality of sections of copper being embedded therein.

23. (New) The semiconductor device of claim 22, wherein said adhesive material comprises tungsten (W).

24. (New) The semiconductive device of claim 20, said third interlayer insulating layer has a hole formed therein, said hole allowing a one of said first plurality of sections of copper to connect with one of said second plurality of sections of copper.